The KM4000 keyer-memory

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Introduction

The KM4000 was originally conceived as an add-on memory unit for existing keyers to fill an obvious need for a mid-range-cost keyer with memory. As the project progressed, however, it became evident that the logic involved in achieving a high degree of reproduction accuracy precluded the concept of an add-on unit. Thus the KM4000 became the first truly low-cost keyer-memory to conform to individual requirements.

The KM4000 was designed with the user in mind and around a well-defined requirement—that it should be a quality product with a realistic price tag. It also had to be a useful addition to amateur radio station equipment without unnecessary frills. From these and many other ideas the essential requirements for the KM4000 became:

1. Single pcb construction.
2. Ease of use.
3. Sufficient storage capability.
4. Iambic or straight paddle keyer operation with dot and dash store.
5. Low cost.
6. High degree of custom flexibility.

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System design

There are two fundamental problems in the operation of the keyer which influence the overall system design. Their solution determines the nature of the circuit elements shown in Fig 1, and ultimately the quality and feel of the final product. First, the keyer must generate morse as an instantaneous response to paddle operation; this implies that it must either be instantaneous by nature, or be seen to be instantaneous by a speedy reaction to morse initiation. Second, the inter-character and inter-word spacings must retain the information imparted as part of the original cw transmission. So the reproduction must be structured in such a way that the spacings are discernible from one another. There are two possible approaches to this problem, each with its own cost penalty, and each influencing the nature of the keyer logic.

The system must either copy the cw exactly as defined by the operator, or automatically generate correct spacings irrespective of any minor variations in the incoming morse. In the second case some form of network to discriminate between the two types of spacing would be needed, along with the ability to represent each as a fixed code. This solution has two advantages over the first: it is likely to make more efficient use of the memory space available, and the reproduced morse will be perfect—provided the original cw is not too distorted. However, the logic involved in performing the space recognition and encoding incurs additional hardware costs which can only be offset by the optimized use of the memory. As the KM4000 is to be a low-cost system with a relatively small information storage capability, this becomes an unattractive solution; a cw copier with a resolution which makes digitizing errors unnoticeable would be best.

This decision influences the choice of the method of governing the keyer response, as it is logical to adopt the same approach as for the memory, and base it on a free-running master clock. So the overall structure of the KM4000 takes the form shown in Fig 1. The next step involves designing logic around this system.

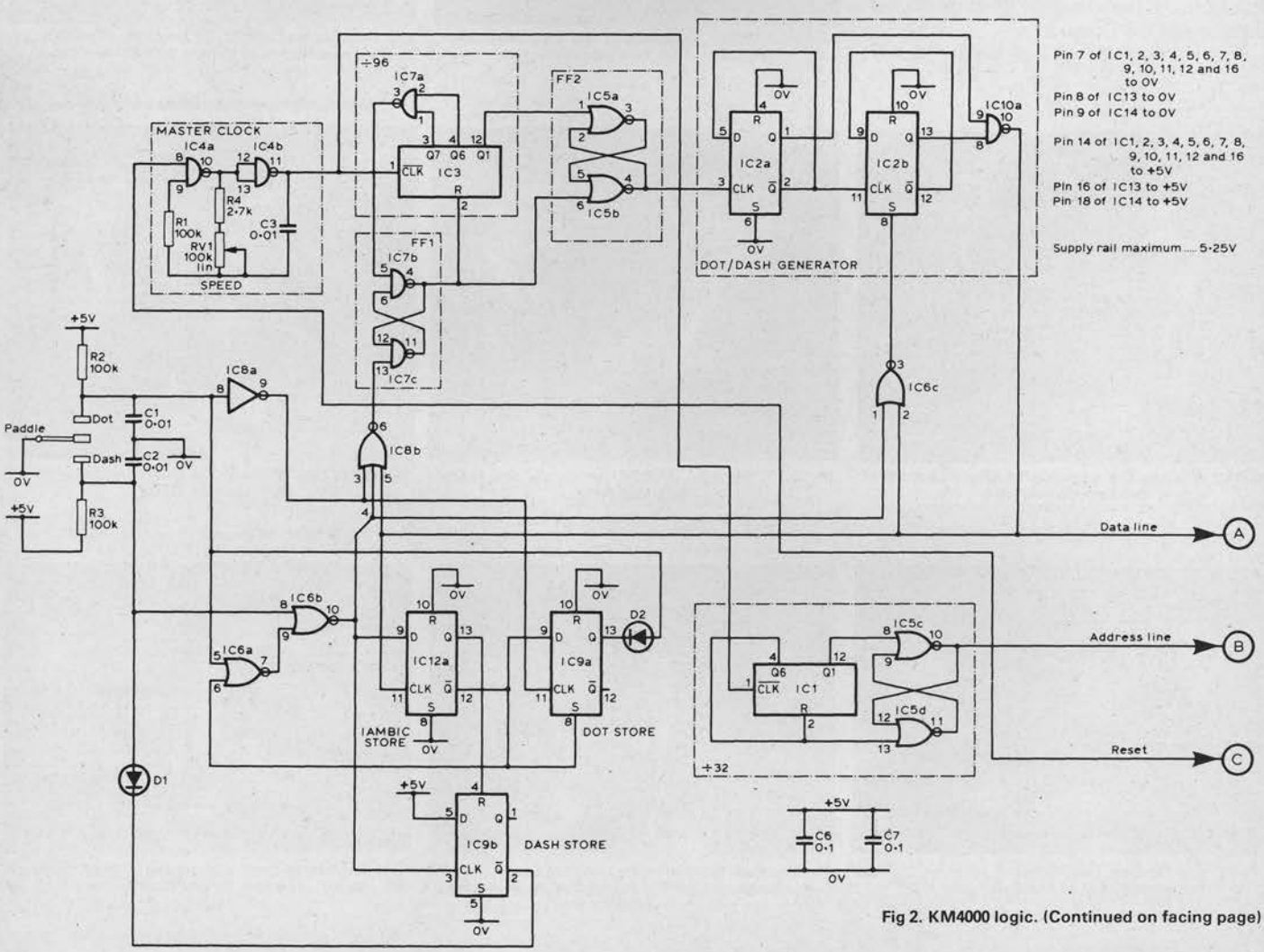


Fig 2. KM4000 logic. (Continued on facing page)

Circuit description

The circuit diagram, Fig 2, shows the KM4000 logic. In order to make description and understanding of the circuit easier it has been drawn in block fashion with well-defined circuit elements referenced *en bloc,* eg IC7B,C is an R–S flip-flop referenced FF1. Broadly speaking the circuit conveniently divides into two main areas: the keyer logic and the memory logic.

The keyer comprises the paddle, dot store, dash store, iambic store, the dot/dash generator and the ÷96 counter. The master clock may be considered as common to the whole system. A dot is sent by keying the paddle to the right, latching FF1 and thereby allowing the ÷96 counter to free-run. Note that by clocking FF2 from the Q1 output, the counter output responds to paddle operation within one clock pulse and the response is seen to be instantaneous. The dot/dash generator is clocked by the positive-going edge from FF2, thus driving data line A high. Since IC2B of the dot/dash generator is held SET by IC6C, the output NAND gate decodes a dot which holds the data line A high for 96 master-clock periods (one dot). A dash is formed in the same way, except

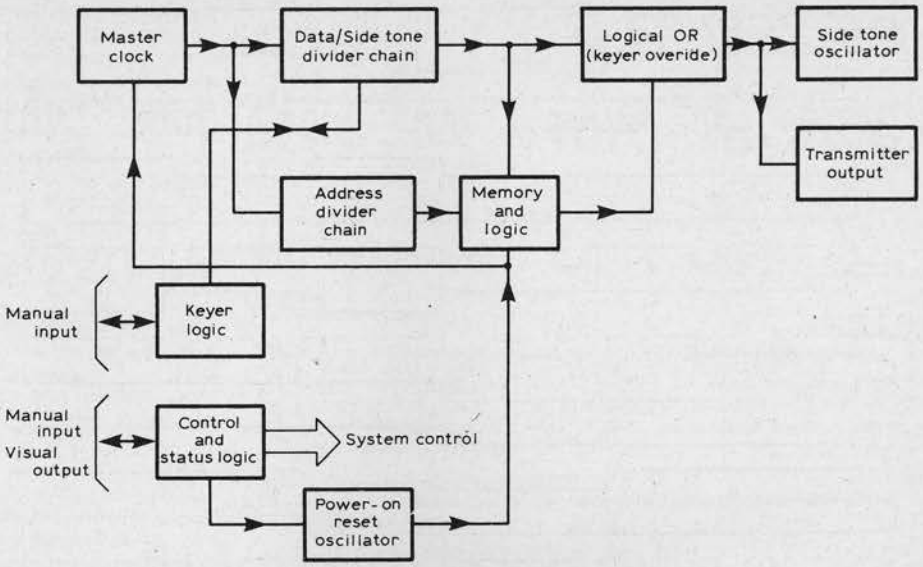
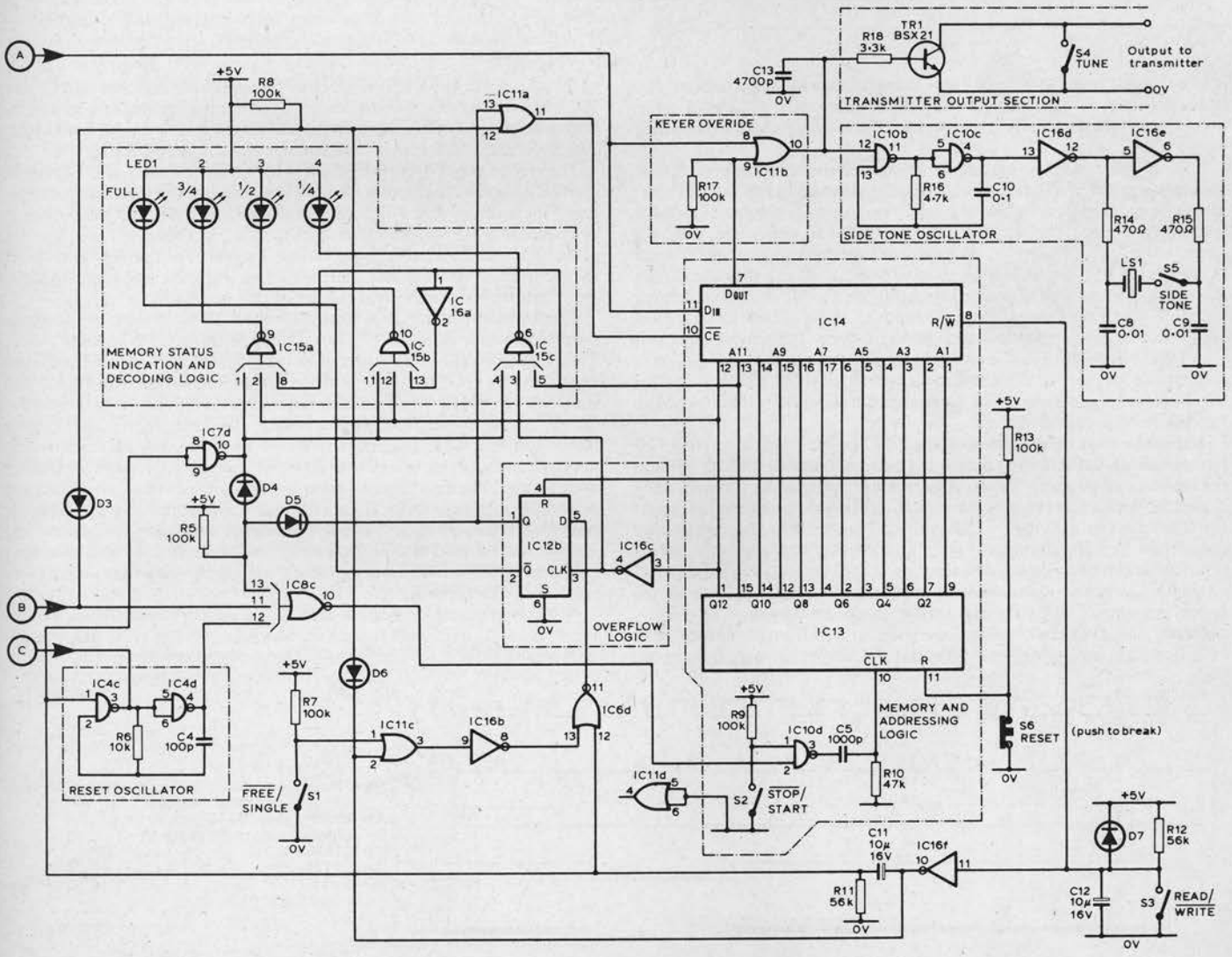


Fig 1. Block diagram, system overview



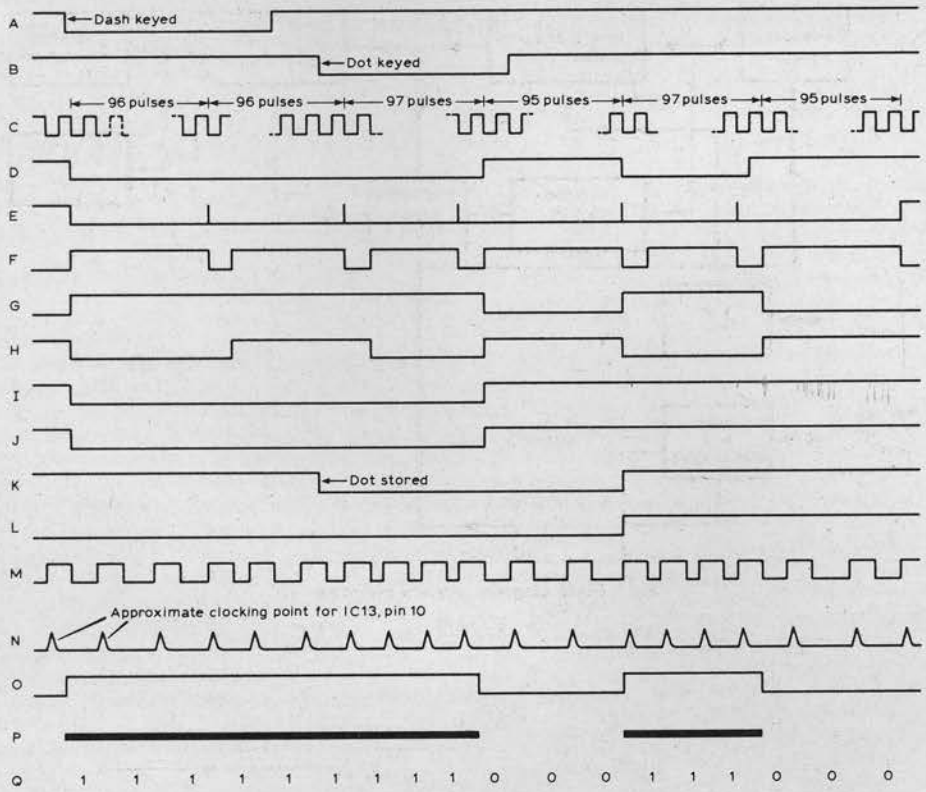


Fig 3. Timing diagram. Writing the letter "N" to the memory showing autospacing dot-store iambic response memory clocking four significant timing waveforms
A = Dash input IC6B pin 8
B = Dot input IC8A pin 8
C = Master clock output IC4B pin 11
D = IC6C pin 3
E = IC7B pin 4 (FF1 output)
F = IC5B pin 4 (FF2 output)
G = Data line "A"
H = IC10A pin 9
I = IC10A pin 8
J = IC9B pin 2
K = IC9A pin 13
L = IC12A pin 12
M = Address line "B" IC5 pin 10
N = Address counter IC13 pin 10
O = IC11B pin 10
P = Morse
Q = Stored data

that in this case both flip-flops are able to toggle; thus the space between two successive dots is filled-in and the output NAND gate decodes a dash. Consequently the dataline is driven high for 3×96 master clock periods (one dash).

In both cases interdigit spacing, ie the space between successive dots or dashes in any one character, is automatically generated as 95 periods long. This is guaranteed by data line A going low—to signify the end of a dot or a dash—one clock period *after* the reset pulse to the $\div 96$. Thus the counter free-runs for another 95 pulses before the next reset pulse from IC7A latches FF1 and holds the counter reset. If at any time during the transmission of a dash the paddle keys a dot, then a "0" is clocked into the dot store which thus ensures that the input of IC8A is kept low after the completion of the current dash and interdigit space. The same technique is used for the dash store but, in this case the $\overline{Q}$ output is used from IC9B to compensate for the "1" clocked into the data input (IC9B pin 5). Note that the diodes on the output of the respective stores perform the logical AND function with the paddle inputs.

The iambic store operates by clocking a "0" (representing a dot) or a "1" (representing a dash) to its Q output in response to the digit which initiates the sequence of dots and dashes. As a result of both paddle contacts being closed the iambic store toggles indefinitely via IC6A, thereby complementing IC6C pin 1 as each digit is transmitted. Thus the first rising edge after completion of a dot disables the SET pin of the dot/dash generator, which results in a dash being decoded by the NAND output gate. As such, a string of alternating dots and dashes is sent, the form of which is defined by the logical sequence in which the paddles are closed and opened.

Finally, the speed at which the morse is sent or read from the memory may be varied from as slow as 2wpm to as fast as 200wpm by varying the speed of the master clock. RV1 is used for this purpose since, together with C3 and R4, it sets the frequency of oscillation, f_o, of the master clock as defined by the equation $f_o = 1 \cdot 4RC$. Incidentally, due to the divider chains used in this design the mark/space ratio of the master clock is not critical.

The second major section of the KM4000 is the memory and associated logic. It comprises the bipolar memory ic and addressing logic, the overflow logic, the memory status indication and decoding logic, and the power-on reset oscillator. These sections are indicated in block form in Fig 2. There is also additional logic performing various ancillary functions; this includes the front-panel switches and interconnecting logic, the side tone oscillator etc. These will be dealt with at the end of this section.

The address counter is a straightforward 12-bit binary counter, the outputs of which drive the 12 address lines on the MM5257 memory chip. Timing considerations associated with the MM5257 require that the $\overline{CE}$ pin be high during positive-going transitions on the address lines, and to this end the clocking waveform to the address counter is modified by the CR network on the output of IC10D (See the timing diagrams, Figs 3 and 4). The bandwidth of this arrangement stretches from the slowest clock speed, approximately 2wpm, to well over 200wpm, and is great enough to cover all eventualities. The data from the keyer is synchronously clocked off data line A into the memory, which is organized as 4,096 words $\times$ 1 bit. Each bit resolves the time-equivalent of one-third dot as defined by the address and data divider ratios. These ratios were arrived at empirically and have been chosen to optimize the memory available while at the same time maintaining resolution and response.

At all times during reading and writing, the memory status is indicated by the 0·25, 0·5, 0·75 and full l.e.ds which are driven from the address decoders IC15 A,B,C. The overflow latch which drives the full l.e.d. is

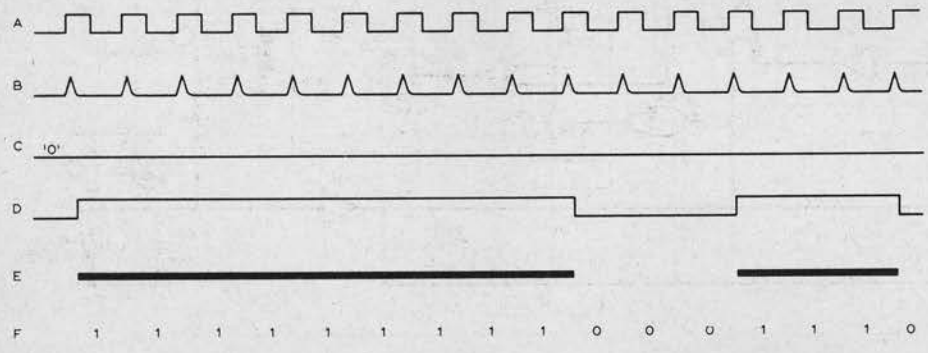


Fig 4. Timing diagram. Reading the letter "N" from the memory
A = Address line "B" IC5 pin 10
B = Address counter IC13 pin 10
C = IC14 Pin 10 $\overline{CE}$
D = IC11 Pin 10
E = Morse
F = Stored data

toggled on the falling edge of Q12 by virtue of inverter IC16C. Therefore it indicates when the memory has just gone into the full state, and prevents data corruption or repetition—when in the write or single read mode respectively—by disabling the memory chip (Q connection to IC11A pin 13) and gating out the address clock (Q connection via D5 to IC8C pin 13).

D4, D5 and R5 perform the logical AND function between the Q output from the overflow latch and the enable line to the power-on reset oscillator via IC7D. When either the overflow latch or IC7D is a "0" IC8C is enabled, thereby allowing either address line B or the reset oscillator to clock the memory. The power-on reset enable line is derived from the differentiator on the output of IC16F. This ensures that:

(a) The memory is cleared for a fixed length of time after power-on irrespective of the read/write switch position.

(b) When S3 is switched to write, the memory is automatically cleared out. This ensures that a short message may be over-recorded on a long message without the remains of the previous message coming through.

(c) The overflow logic (See Fig 2) is disabled during reset (connection via IC6D pin 12 to IC12B pin 5) which allows several memory reset cycles to be made.

(d) The l.e.ds are also held off by means of IC7D.

During power-on reset the memory is held in the write condition for approximately 560ms as defined by the RC time constant of R12, C12. D7 acts as a discharge path for C12 when the +5V rail is powered down.

In the free-run mode IC6D disables the overflow logic and allows the data to be cyclically read out. However, the free-run action is prevented in the write mode (IC16F connection to IC11C pin 2) irrespective of the free/single switch position, guaranteeing that data corruption through over-recording is not possible.

Data output from the memory is ORed with the data line A, allowing the keyer to be used irrespective of the state of the rest of the system. Coupled with the stop/start switch which halts memory operation, this enables the operator to make an immediate response to any incoming cw when full break-in mode is used, providing a very powerful override facility. The resulting output from IC11B drives the sidetone oscillator and the transmitter output. In the standard KM4000 a BSX21 is used in the TR1 position. This has a worst-case h_{FE} of 40 and a breakdown V_{CEO} of 120V. The cmos OR gate IC11B is capable of supplying approximately 1mA base drive, so enabling TR1 to sink a maximum of 40mA. This should suffice for most transmitters. Any equipment which exceeds these parameters will require that TR1 be changed or relay switches be used. S4 across the transmitter output has been included to facilitate tuning the transmitter.

The choice of psu for the KM4000 is largely up to the individual but should be capable of supplying 80mA at +5V dc. The bulk of this current is consumed by the memory ic which, being bipolar, dictates that the supply should also be regulated to ±0·25V. Although a battery back-up is somewhat impracticable with this level of current consumption, it could be included to prevent volatility over short periods of time. The memory ic will retain preprogrammed data down to a V_{CC} of +2V. For those who do not wish to supply their own psu, a suitable design is shown in Fig 5. The voltage regulator used here has internal foldback, overload, thermal and short-circuit protection and regulates 100mA at +5V. The psu pcb is given in Figs 6, 7 and 8. Finally, the push-to-break reset switch sets all address lines to zero for a memory read or write.

Construction

Because this design is user-definable, planning the construction and deciding upon the mechanical layout lies in the hands of the constructor. However, in common with most electronic projects there are guidelines which, if followed, simplify construction of a neat and professional-looking piece of equipment. The following guidelines also include comments specific to the KM4000.

Before assembling any components on the pcb it is advisable to lay the board on a piece of paper and mark out a template so that its mounting holes

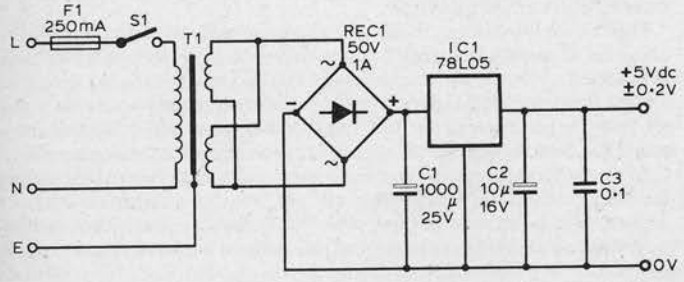


Fig 5. PSU circuit diagram

Components list

KM4000

R1, 2, 3, 5, 7, 8, 9, 13, 17	100kΩ ±5%	**C1, 2, 3, 8, 9**	0·01μF Mullard 352 series
R4	2·7kΩ ±5%	**C4**	100pF disc cer (min)
R6	10kΩ ±5%	**C5**	1,000pF disc cer (min)
R10	47kΩ ±5%	**C6, 7, 10**	0·1μF Mullard 352 series
R11, 12	56kΩ ±5%	**C11, 12**	10pF 16V rad
R14, 15	470kΩ ±5%	**C13**	4,700pF min plate cer
R16	4·7kΩ ±2%	**D1-7**	General purpose silicon
R18	3·3kΩ ±5%	**TR1**	BSX21 (see text)
(All resistors 0·25W)			
RV1	100kΩ linear	**LED 1-4**	3mm red
		LS1	Piezo cer transducer

(For speed 8-32wpm 50kΩ linear plus 15kΩ ±5% in series)

IC1, 3	4024B cmos	**IC11**	4017B cmos
IC2, 9, 12	4013B cmos	**IC13**	4040B cmos
IC4, 7, 10	4011B cmos	**IC14**	MM5257 memory
IC5, 6	4001B cmos	**IC15**	4023B cmos
IC8	4000B or 4025B cmos	**IC16**	4069B cmos

(IC socket: Soldercon ic socket pins (if required))

S1-5	Miniature toggle spst
S6	Miniature push-button, momentary action, one normally closed contact
Veropins	Half-pin (18)
Track pins	T1558-01 (42)

PSU FOR KM4000

C1	1,000μF 25V 7·5mm lead space	**T1**	0-6V L3VA 196-296
C2	10μF 16V rad	**REC1**	Bridge 50V 1A 262-141
C3	0·1μF Mullard 352 series	**S1**	SPST 250V ac
IC1	78LO5 100mA regulator	**F1**	250mA
		Veropins	Half-pin (4)

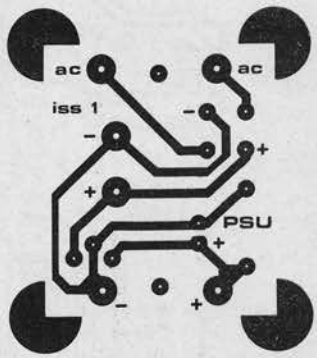


Fig 6. PSU pcb

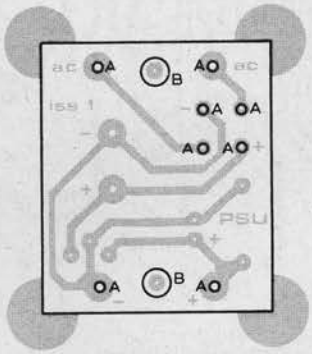


Fig 7. PSU pcb drilling plan

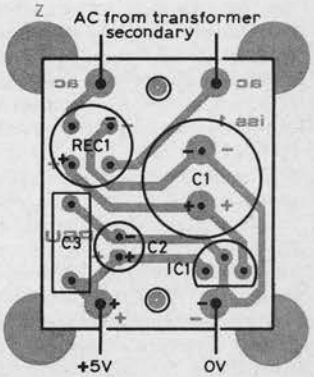


Fig 8. PSU component layout

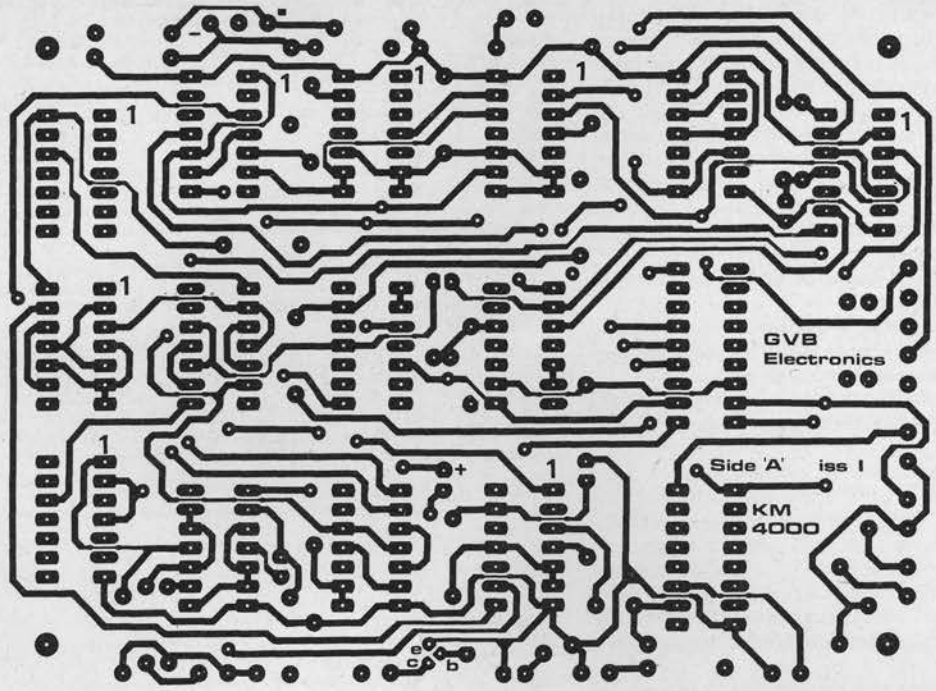


Fig 9. KM4000 pcb side "A"

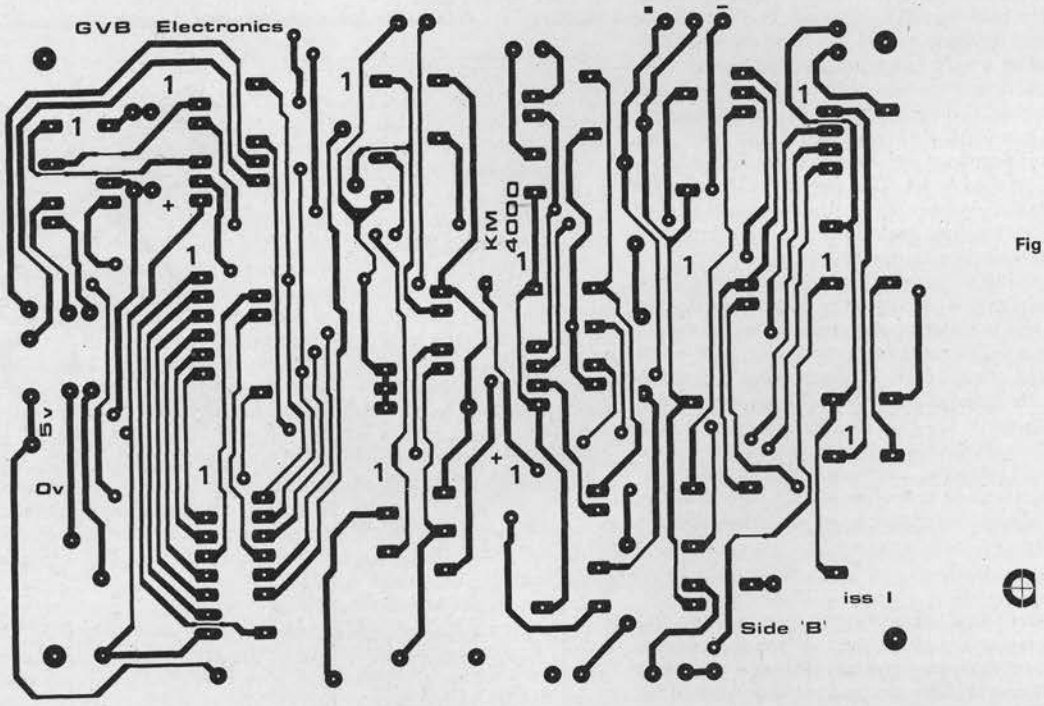


Fig 10. KM4000 pcb side "B"

may be accurately located when the unit is finally mounted in a box. Alternatively, if an enclosure has already been purchased the positions may be marked off directly. The pcb has been predrilled for 3mm (6BA) mounting studs. Next, carry out a visual check of the pcb prior to construction to ensure that the board has not been damaged in transit—this check may prove invaluable later on. The pcb artwork is shown in Figs 9, 10, 11 and 12.

The pcb has been laid out to minimize top soldering and pinning, and should present no problems to most constructors. The smallest soldering iron bit available should be used and after each component has been inserted check for any missed connections. As a rule of thumb the board should be assembled by starting with the lowest profile components and working up to the highest. The general assembly is shown in Fig 12.

Begin by inserting all the pcb pins in the positions marked in Fig 12. Some of these are located under ics, so ensure that none is missed and that they do not stick up too high after soldering. The through-hole pin used on the prototype is the Harwin T1558-01, which is supplied in the very convenient form of each pin connected top to tip—making it an easy matter to insert the end pin and break it free. However, 22swg tinned wire may be used instead. There are 42 pins in all.

Then insert the diodes, observing the correct polarity, and the resistors. These are all set on a 0·4in pitch and may thus be correctly preformed prior to insertion.

Next, insert the 25 board pins which connect to the psu, switches, l.e.ds etc, from the perimeter of the pcb. Standard Veropins can be used here as the board has been drilled out to 1mm in these positions. At this point the ics should be soldered into their respective locations, taking care to follow cmos handling precautions. Ensure that correct polarity is observed—the pcb has been laid out so that pin 1 uniformly lies in the same direction for all ics. Note that ic sockets cannot be used on this pcb as it is necessary to top solder the ics.

Follow up with the small capacitors, the transmitter output transistor and

Table 1
Speed related memory times

WPM	Seconds	WPM	Seconds
6	290	40	43
9	193	60	29
12	145	100	17·4
15	116	150	11·6
20	87	200	8·7
30	58		

The word storage capacity based upon the "standard" word *PARIS* is 29 words. The wpm speeds have been based on this standard.

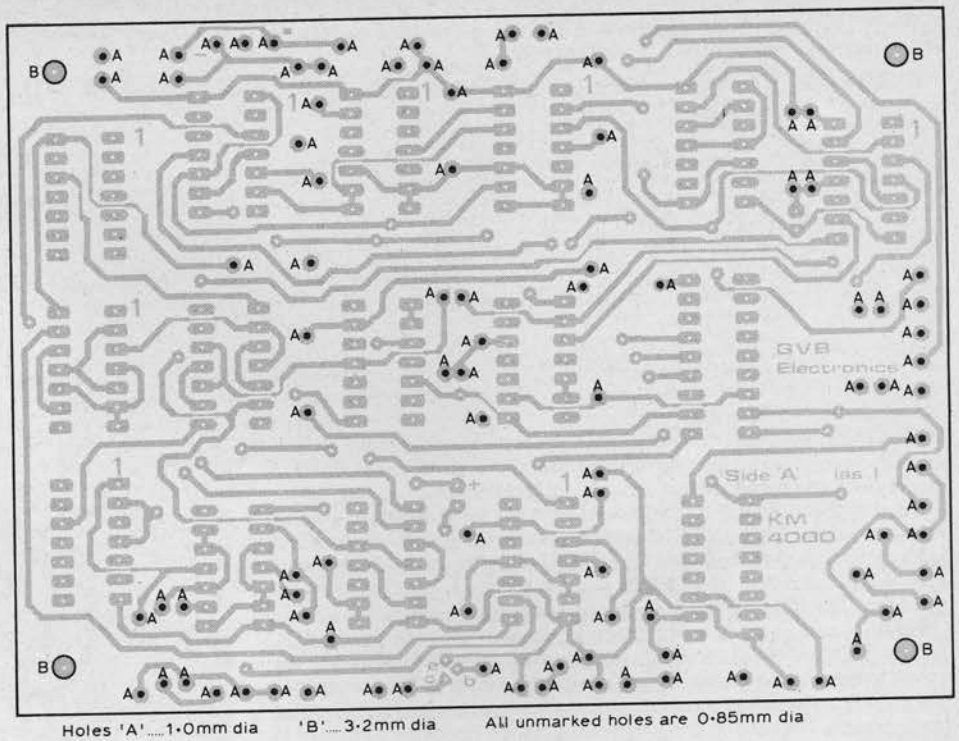


Fig 11. KM4000 pcb drilling plan

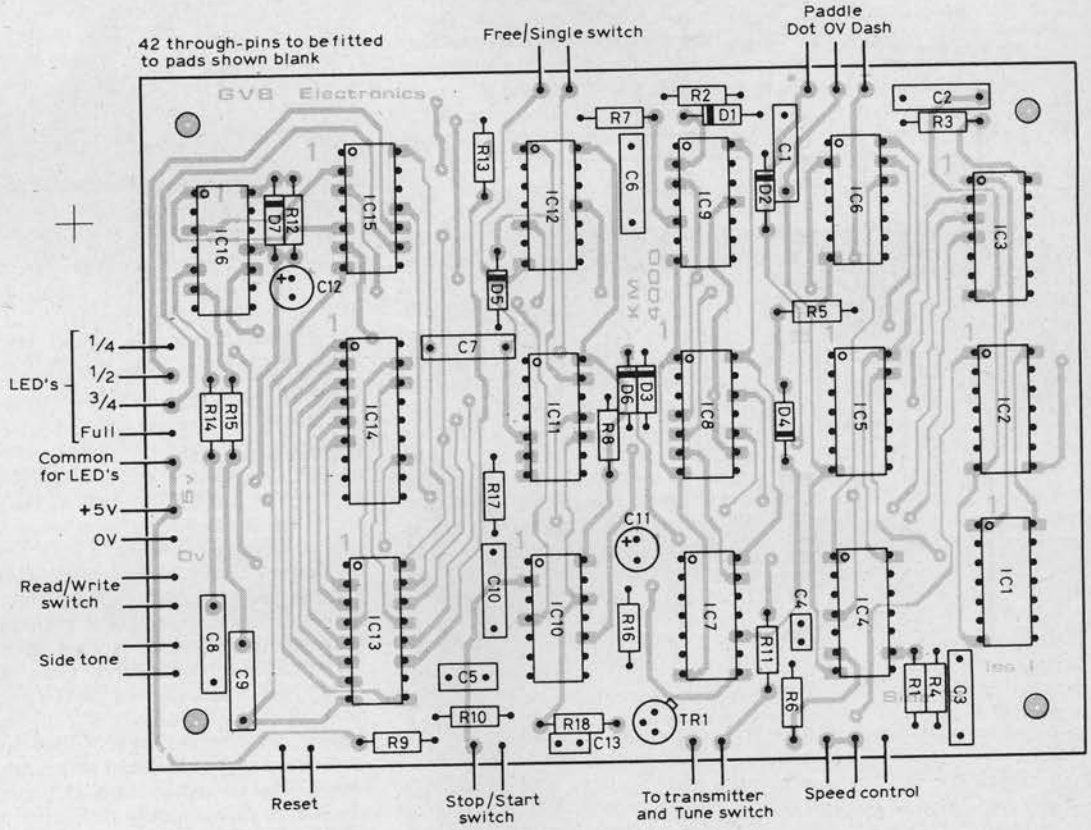


Fig 12. KM4000 component layout

the large capacitors. The positive leads of both electrolytics are marked with a + sign on the pcb, and the transistor legs have the collector and base positions marked c and b respectively.

Having inserted the components, the remaining top-side pads should now be soldered.

All that remains is to fit the completed board, psu and one's favourite paddle into the chosen box. The l.e.ds, switches and RV1 may be arranged on the front panel as desired. Incidentally, convention dictates that the paddle should be wired dots to the right, dashes to the left, so it is a good idea to follow this standard when wiring in the paddle. If it is decided not to fit any of the front-panel switches that have been allowed for, it is not necessary to wire out these positions on the pcb. The default case where any switch is omitted is catered for by the logic.

Using the KM4000

Begin by applying power to the KM4000 while monitoring the supply current. Typically this should be 35–40mA, but a tolerance weighting could take this as high as 80mA. Any l.e.d. indication at this point should be ignored.

Check that the keyer section and sidetone oscillator are functional by

Table 2. Logical interdependence of the front panel switches

Stop/Start	Read/Write	Reset	Free/Single	Comments
Stop	Don't care	Don't care	Don't care	Keyer functions memory halted
Start	Write	Reset	Don't care	Memory loads data from keyer
Start	Write	Reset	Don't care	Resets memory
Start	Read	Reset	Free	Reads out data cyclically
Start	Read	Reset	Single	Reads out data once
Start	Read	Reset	Don't care	No output from memory Allows keyer to over-ride

keying morse at different speeds and making sure that the dot and dash stores operate correctly—these are best checked at the slowest speed at which the keyer will run. To write to the memory, switch into the write mode and press RESET. When the reset button is released the memory immediately starts to clock in data from the keyer and will continue to do so until the full l.e.d. is lit. The 0·25, 0·5 and 0·75 l.e.ds provide a visual indication of memory breakpoints and will light up in sequence as the memory gradually fills up. To read the message, switch to READ and press the reset button. The KM4000 will respond by retransmitting the stored message at the same speed. Note that the information capacity does not vary with the speed of the master clock and remains constant under all conditions.

Based on the accepted "standard word" *PARIS* the KM4000 has a word-storage capacity of 29 words. The speed may be varied by altering the setting of RV1 which, as a result, will vary the length of time over which the message is transmitted, see Table 1. Thus in the free-run mode with a fast replay speed the KM4000 may be used for meteor scatter work. Other uses include CQ calls, morse practice, and callsign generation—write in the callsign, say, every 20s or so until the memory is full, select free-run (S1) and take the output to the microphone socket of the transmitter via a "T" pad attenuator (see Fig 13), or indeed to a tape recorder to facilitate the making of morse practice tapes. The logical interdependence of the front-panel switches is shown in Table 2.

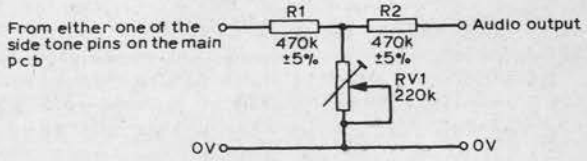


Fig 13. "T" pad attenuator

The quality of the sidetone oscillator is important in any keyer, and the piezo-ceramic device used in this design is associated with the shaping network IC16D, E, R14, R15, C8 and C9. This removes some of the harmonics that tend to give it a harsh quality when driven by a square wave and results in a more mellow tone. However, there is much room for experimentation in this area, and a great deal can be achieved by modifying the resonant cavity in which the transducer is housed. Broadly speaking, increasing the depth of the port and the cavity volume tends to decrease the resonant frequency, whereas decreasing the area of the port tends to increase it. Ideally the piezo transducer should be driven by a sine wave as this results in a soft, mellow tone. However, in order to get a reasonable volume with a sine wave the peak-to-peak voltage needs to be much higher than is possible with a +5V rail. Incidentally, other devices such as crystal earpieces have also been used on the prototype with good results. The sidetone frequency is set by R16, C10, and for the values shown in Fig 2 it is approximately 1kHz.

Conclusion

In practice the KM4000 has proved easy to use; it has succeeded in satisfying the performance required of it and has met an enthusiastic reception among local radio amateurs. A number have already been built and all have worked first time. PCBs are available exclusively for £9.62, incl p&p, from GVB Electronics, 95 Old Worthing Road, East Preston, West Sussex BN16 1DU; tel 09062 70260. Alternatively, a ready-built and tested board will be supplied for £44.95, incl p&p.

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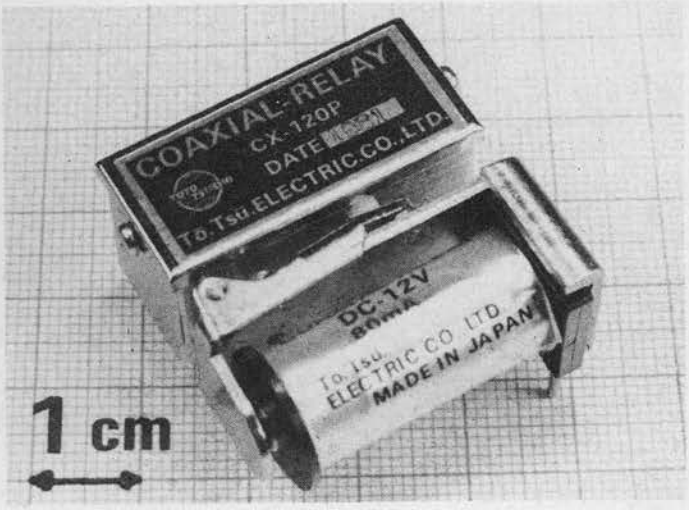
NEW PRODUCTS

Toyo-Tsusho CX120P coaxial relay

The versatile CX120P coaxial relay is one of a comprehensive range of pcb-mounting devices made by this manufacturer. It has an exceptionally low vswr to over 1GHz, and crosstalk is better than 80dB across the hf range —and it is still better than 50dB at uhf frequencies.



The CX120P coaxial relay

An insertion loss of only 0·2dB at 2·5GHz, and the pcb terminations, make it a most versatile antenna relay. Applications include remote antenna switching, power attenuator switching, transceiver antenna changeover, and antenna grounding systems.

For further information contact Ambit International, 200 North Service Road, Brentwood, Essex CM14 4SG; tel 0277 230909.

Barrie's toroids

Barrie Electronics Ltd can now supply toroidal transformers, rated at 30, 60, 100, 160, 230, 330 and 530VA. The primary 110, 220 or 240V windings and the dual secondaries, in a range from 6+6 to 50+50V, have been selected to meet the needs of both professional electrical and electronic engineers and DIY enthusiasts. From a list of 58 toroidal transformers; it is possible to cover most requirements because the secondaries can be connected in series, parallel or independently. Each transformer is tested between primary to secondary insulation at 4kV.

The toroidal transformers, from the Cotswold Electronics "budget range", will complement the 150 laminated types held by Barrie Electronics, on an off-the-shelf basis, and will provide a range of transformers which are 50 per cent lighter and 50 per cent lower volume, and with a very low height to diameter ratio, compared with stacked laminated types, which makes toroids ideal for use in "slim-line" electronics. The toroidal transformer also has an approximately 10:1 better radiated noise (hum) characteristic and is acoustically quieter, which gives greater latitude when siting the transformer.

Each transformer is supplied with a data sheet giving technical details on the operation and installation of the Cotswold toroids. The grain oriented silicon steel clockspring cores permit operation at high flux density, with very low iron losses, resulting in high efficiency. Although the toroids in the "budget range" are designed to be operated within specific load, regulation and temperature rise parameters, they can also be used in a "derated" condition at a lower temperature rise and with improved regulation without incurring too much of a size penalty.

For further information contact Barrie Electronics Ltd, 3 The Minories, London EC3N 1BJ; tel 01-488 3316-7-8.